CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

A1> 1. A programming circuit for a plurality of programmable elements, said programming circuit comprising:

a plurality of programmable elements;

a plurality of element programming circuits each associated with a programmable element and each including a latch circuit for receiving and holding a desired programming state of an associated programmable element, said plurality of element programming circuits setting the state of said associated programmable elements in accordance with a desired programming state held in an associated latch in response to a common control signal.

2. A circuit as in claim 1, wherein each said latch circuit comprises:

an inverter circuit having an input coupled to an input of said latch circuit and an output coupled to an output of said latch circuit;

a pair of n-channel transistors connected in series between an input of said latch circuit and a first reference voltage;

a pair of p-channel transistors connected in parallel between said input of said latch circuit and a second reference voltage;

a read-and-latch signal line coupled to control gates of a first of said pair of p-channel transistors and a first of said pair of n-channel transistors;

wherein said output of said inverter circuit is coupled to control gates of a second of said pair of p-channel transistors and a second of said pair of n-channel transistors.

3. A circuit as in claim 2, wherein said read-and-latch signal line is configured to apply a read-and-latch signal to permit reading and latching of said desired programming signal.

4. A circuit as in claim 2, wherein a third p-channel transistor is coupled between said pair of parallel-connected p-channel transistors and said second reference voltage, said third p-channel transistor having a gate coupled to said first reference voltage.

5. A circuit as in claim 1, wherein said common control signal includes a voltage of between approximately 8 and 9 volts.

6. A circuit as in claim 1, wherein said common control signal includes a voltage sufficient to change a state of said associated programmable elements.

42 7. A programming circuit for a programmable element, comprising:

at least one latch circuit;

at least one latch-programming circuit for temporarily applying a programming signal to an input of a respective latch circuit, said latch circuit latching a state of said programming signal;

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a signal line applying a voltage sufficient to change the state of said programmable element;

at least one latch isolation transistor coupled between said programmable element and said latch circuit;

at least one state control transistor coupled between said programmable element and a first reference voltage and having a gate controlled by an output of said latch circuit;

wherein during a programming phase, said latch circuit is configured to latch said programming signal, and during a common control phase, said latch isolation transistor is configured to decouple said programmable element from said latch circuit and said signal line is configured to apply said state-changing voltage to said programmable element if said output of said latch circuit turns on said state control transistor.

8. A circuit as in claim 7, wherein said at least one latch circuit comprises:

an inverter circuit having an input coupled to said input of said latch circuit and an output coupled to said output of said latch circuit;

a pair of n-channel transistors connected in series between an input of said latch circuit and said first reference voltage;

a pair of p-channel transistors connected in parallel between said input of said latch circuit and a second reference voltage;

a read-and-latch signal line coupled to control gates of a first of said pair of p-channel transistors and a first of said pair of n-channel transistors;

wherein said output of said inverter circuit is coupled to control gates of a second of said pair of p-channel transistors and a second of said pair of n-channel transistors.

9. A circuit as in claim 8, wherein said read-and-latch signal line is configured to apply a read-and-latch signal during said programming phase to permit reading and latching of said programming signal.

10. A circuit as in claim 8, wherein a third p-channel transistor is coupled between said pair of parallel-connected p-channel transistors and said second reference voltage, said third p-channel transistor having a gate coupled to said first reference voltage.

11. A circuit as in claim 7, further comprising at least one programming enable transistor configured to couple said state control transistor to said programmable element during said common control phase.

12. A circuit as in claim 7, further comprising at least one programmable element isolation transistor configured to decouple said programmable element from said latch circuit and said latch-programming circuit during said programming phase.

13. A circuit as in claim 7, wherein said latch-programming circuit comprises at least one latch-programming transistor having a gate controlled by a first latch-programming signal, a first source/drain coupled to a second latch-programming signal, and a second source/drain coupled to said input of said latch circuit through said latch isolation transistor.

14. A circuit as in claim 7, wherein during said common control phase, said state-changing voltage of between approximately 8 and 9 volts is applied to said signal line.

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15. A circuit as in claim 7, wherein said state-changing voltage includes a voltage sufficient to blow an anti-fuse.

A3 16. A memory circuit, comprising:

a plurality of memory elements; and

at least one programming circuit associated with a plurality of programmable elements and configured to activate one or more of said plurality of memory elements, said programming circuit comprising:

a plurality of programmable elements;

a plurality of element programming circuits each associated with a programmable element and each including a latch circuit for receiving and holding a desired programming state of an associated programmable element, said plurality of element programming circuits setting the state of said associated programmable elements in accordance with a desired programming state held in an associated latch in response to a common control signal.

17. A memory circuit as in claim 16, wherein each said latch circuit comprises:

an inverter circuit having an input coupled to an input of said latch circuit and an output coupled to an output of said latch circuit;

a pair of n-channel transistors connected in series between an input of said latch circuit and a first reference voltage;

a pair of p-channel transistors connected in parallel between said input of said latch circuit and a second reference voltage;

a read-and-latch signal line coupled to control gates of a first of said pair of p-channel transistors and a first of said pair of n-channel transistors;

wherein said output of said inverter circuit is coupled to control gates of a second of said pair of p-channel transistors and a second of said pair of n-channel transistors.

18. A memory circuit as in claim 17, wherein said read-and-latch signal line is configured to apply a read-and-latch signal to permit reading and latching of said desired programming signal.

19. A memory circuit as in claim 17, wherein a third p-channel transistor is coupled between said pair of parallel-connected p-channel transistors and said second reference voltage, said third p-channel transistor having a gate coupled to said first reference voltage.

20. A memory circuit as in claim 16, wherein said common control signal includes a voltage of between approximately 8 and 9 volts.

21. A memory circuit, comprising:

a plurality of memory elements; and

at least one programming circuit associated with a plurality of programmable elements and configured to activate one or more of said plurality of memory elements, said programming circuit comprising:

at least one latch circuit;

at least one latch-programming circuit for temporarily applying a programming signal to an input of a respective latch circuit, said latch circuit latching a state of said programming signal;

Add Cont. a signal line applying a voltage sufficient to change the state of said programmable element;

at least one latch isolation transistor coupled between said programmable element and said latch circuit;

at least one state control transistor coupled between said programmable element and a first reference voltage and having a gate controlled by an output of said latch circuit;

wherein during a programming phase, said latch circuit is configured to latch said programming signal, and during a common control phase, said latch isolation transistor is configured to decouple said programmable element from said latch circuit and said signal line is configured to apply said state-changing voltage to said programmable element if said output of said latch circuit turns on said state control transistor.

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22. A memory circuit as in claim ~~21~~, wherein said at least one latch circuit comprises:

an inverter circuit having an input coupled to said input of said latch circuit and an output coupled to said output of said latch circuit;

a pair of n-channel transistors connected in series between an input of said latch circuit and said first reference voltage;

a pair of p-channel transistors connected in parallel between said input of said latch circuit and a second reference voltage;

a read-and-latch signal line coupled to control gates of a first of said pair of p-channel transistors and a first of said pair of n-channel transistors;

wherein said output of said inverter circuit is coupled to control gates of a second of said pair of p-channel transistors and a second of said pair of n-channel transistors.

23. A memory circuit as in claim 22, wherein said read-and-latch signal line is configured to apply a read-and-latch signal during said programming phase to permit reading and latching of said programming signal.

24. A memory circuit as in claim 22, wherein a third p-channel transistor is coupled between said pair of parallel-connected p-channel transistors and said second reference voltage, said third p-channel transistor having a gate coupled to said first reference voltage.

25. A memory circuit as in claim ~~21~~ 20, further comprising at least one programming enable transistor configured to couple said state control transistor to said programmable element during said common control phase.

26. A memory circuit as in claim ~~21~~ 20, further comprising at least one programmable element isolation transistor configured to decouple said programmable element from said latch circuit and said latch-programming circuit during said programming phase.

27. A memory circuit as in claim 21, wherein said latch-programming circuit comprises at least one latch-programming transistor having a gate controlled by a first latch-programming signal, a first source/drain coupled to a second latch-programming signal, and a second source/drain coupled to said input of said latch circuit through said latch isolation transistor.

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~~28~~. A memory circuit as in claim ~~21~~, wherein during said common control phase, said state-changing voltage of between approximately 8 and 9 volts is applied to said signal line.

29. A processor system, comprising:

a processor;

at least one memory device coupled to said processor and including at least one programming circuit, said programming circuit comprising:

a plurality of programmable elements;

a plurality of element programming circuits each associated with a programmable element and each including a latch circuit for receiving and holding a desired programming state of an associated programmable element, said plurality of element programming circuits setting the state of said associated programmable elements in accordance with a desired programming state held in an associated latch in response to a common control signal.

30. A system as in claim 29, wherein each said latch circuit comprises:

an inverter circuit having an input coupled to an input of said latch circuit and an output coupled to an output of said latch circuit;

a pair of n-channel transistors connected in series between an input of said latch circuit and a first reference voltage;

a pair of p-channel transistors connected in parallel between said input of said latch circuit and a second reference voltage;

a read-and-latch signal line coupled to control gates of a first of said pair of p-channel transistors and a first of said pair of n-channel transistors;

wherein said output of said inverter circuit is coupled to control gates of a second of said pair of p-channel transistors and a second of said pair of n-channel transistors.

31. A system as in claim 30, wherein said read-and-latch signal line is configured to apply a read-and-latch signal to permit reading and latching of said desired programming signal.

32. A system as in claim 30, wherein a third p-channel transistor is coupled between said pair of parallel-connected p-channel transistors and said second reference voltage, said third p-channel transistor having a gate coupled to said first reference voltage.

33. A system as in claim 29, wherein said common control signal includes a voltage of between approximately 8 and 9 volts.

34. A processor system, comprising:

a processor;

at least one memory device coupled to said processor and including at least one programming circuit, said programming circuit comprising:

at least one latch circuit;

at least one latch-programming circuit for temporarily applying a programming signal to an input of a respective latch circuit, said latch circuit latching a state of said programming signal;

a signal line applying a voltage sufficient to change the state of said programmable element;

at least one latch isolation transistor coupled between said programmable element and said latch circuit;

at least one state control transistor coupled between said programmable element and a first reference voltage and having a gate controlled by an output of said latch circuit;

wherein during a programming phase, said latch circuit is configured to latch said programming signal, and during a common control phase, said latch isolation transistor is configured to decouple said programmable element from said latch circuit and said signal line is configured to apply said state-changing voltage to said programmable element if said output of said latch circuit turns on said state control transistor.

35. A system as in claim 34, wherein said at least one latch circuit comprises:

an inverter circuit having an input coupled to said input of said latch circuit and an output coupled to said output of said latch circuit;

a pair of n-channel transistors connected in series between an input of said latch circuit and said first reference voltage;

a pair of p-channel transistors connected in parallel between said input of said latch circuit and a second reference voltage;

a read-and-latch signal line coupled to control gates of a first of said pair of p-channel transistors and a first of said pair of n-channel transistors;

wherein said output of said inverter circuit is coupled to control gates of a second of said pair of p-channel transistors and a second of said pair of n-channel transistors.

36. A system as in claim 35, wherein said read-and-latch signal line is configured to apply a read-and-latch signal during said programming phase to permit reading and latching of said programming signal.

37. A system as in claim 35, wherein a third p-channel transistor is coupled between said pair of parallel-connected p-channel transistors and said second reference voltage, said third p-channel transistor having a gate coupled to said first reference voltage.

38. A system as in claim 34, further comprising at least one programming enable transistor configured to couple said state control transistor to said programmable element during said common control phase.

39. A system as in claim 34, further comprising at least one programmable element isolation transistor configured to decouple said programmable element from said latch circuit and said latch-programming circuit during said programming phase.

40. A system as in claim 34, wherein said latch-programming circuit comprises at least one latch-programming transistor having a gate controlled by a first latch-programming signal, a first source/drain coupled to a second latch-programming signal, and a second source/drain coupled to said input of said latch circuit through said latch isolation transistor.

41. A system as in claim 34, wherein during said common control phase, said state-changing voltage of between approximately 8 and 9 volts is applied to said signal line.

42. A system as in claim 34, wherein said processor and said memory device are on a same integrated circuit chip.

43. A method of programming a plurality of programmable elements, comprising:

soft-programming a plurality of latches to a desired state, each latch associated with a respective programmable element; and

hard-programming said plurality of programmable elements with said state of an associated latch using a common control signal.

44. A method as in claim 43, further comprising:

providing a plurality of state control transistors each coupled between a respective programmable element and a first reference voltage;

during a programming phase, applying a programming signal to an input of said latches, and latching said programming signal in each said latch circuit;

during a common control phase, decoupling said programmable element from said latch circuit using a latch isolation transistor and applying a voltage sufficient to change a state of said programmable element if an output of said latch circuit activates said state control transistor.

45. A method as in claim 44, wherein said latching of said programming signal includes applying a read-and-latch signal to said latch circuit.

46. A method as in claim 44, further comprising coupling said programmable element to said state control transistor by activating a gate of a programming enable transistor during said common control phase.

47. A method as in claim 44, further comprising decoupling said programmable element from said latch circuit and said state control transistor during said programming phase.

48. A method as in claim 44, wherein said applying of said programming signal includes controlling a gate of a latch programming transistor using a first latch programming signal line and coupling a second latch programming signal line to said input of said latch circuit through said latch programming transistor.

49. A method as in claim 44, wherein said common control signal includes a voltage of between approximately 8 and 9 volts.

50. A method of programming a programmable element, comprising:

providing a state control transistor coupled between said programmable element and a first reference voltage;

providing a latch circuit having an input coupled to said programmable element through a latch isolation transistor and an output coupled to control a gate of said state control transistor;

during a programming phase, applying a programming signal to said input of said latch circuit, and latching said programming signal in said latch circuit;

during a common control phase, applying a voltage sufficient to change a state of said programmable element if an output of said latch circuit activates said state control transistor, and decoupling said programmable element from said latch circuit using said latch isolation transistor.

51. A method as in claim 50, wherein said latching of said programming signal includes applying a read-and-latch signal to said latch circuit.

52. A method as in claim 50, further comprising coupling said programmable element to said state control transistor by activating a gate of a programming enable transistor during said common control phase.

53. A method as in claim 50, further comprising decoupling said programmable element from said latch circuit and said state control transistor during said programming phase.

54. A method as in claim 50, wherein said applying of said programming signal includes controlling a gate of a latch programming transistor using a first latch programming signal line and coupling a second latch programming signal line to said input of said latch circuit through said latch programming transistor.

55. A method as in claim 50, wherein said applying of said state changing voltage includes applying a voltage of between approximately 8 and 9 volts to said programmable element using a common control signal line.